Greatly Improved 3C-SiC p-n Junction Diodes Grown by Chemical Vapor Deposition

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Abstract—**In this paper we report on the fabrication and initial electrical characterization of greatly improved 3C-SiC (β-SiC) p-n junction diodes. These diodes, which were grown on commercially available 6H-SiC substrates by chemical vapor deposition, demonstrate rectification to −200 V at room temperature, representing a fourfold improvement in reported 3C-SiC diode blocking voltage. The reverse leakage currents and saturation current densities measured on these diodes also show significant improvement compared to previously reported 3C-SiC p-n junction diodes. When placed under sufficient forward bias, the diodes emit significantly bright green–yellow light. These results should lead to substantial advancements in 3C-SiC transistor performance.**

In recent years there has been increasing interest and research into silicon carbide (SiC) as a semiconductor for use in high-temperature, high-power, and/or high-radiation operating conditions under which silicon and conventional III–V semiconductors cannot adequately function. Of the two most common SiC polytypes investigated to date (6H-SiC and 3C-SiC), the 6H polytype has clearly yielded far superior electrical device results. However, this is almost entirely due to the fact that growth techniques for producing substrates and epitaxial films in the 6H material are well advanced compared to 3C-SiC substrate and epitaxial film growth methods [1]–[3].

3C-SiC has some important material property advantages over 6H-SiC, such as higher low-field electron mobility, which could be exploited to produce superior devices and circuits for microwave power and other applications [4]–[6]. Because no technique has been developed for obtaining semiconductor device quality 3C-SiC on suitably large substrates, these property advantages have not been realized in electrical devices or circuits. Given the lack of 3C substrates suitable for mass production, efforts have focused on heteroepitaxial growth of 3C-SiC layers on silicon and other potentially large-area reproducible substrate materials. To date, however, the crystallographic quality of the 3C-SiC resulting from these efforts has been poor, containing high densities of stacking faults, double-positioning boundaries (DPB's), microtwins, threading dislocations, and other undesirable crystal defects [7]–[9]. These defects manifest themselves in the poor electrical characteristics of diodes and transistors fabricated in the resulting 3C-SiC material. Diode junctions at room temperature have been very leaky, exhibiting milliampere per square centimeter current densities at less than 10-V reverse bias. The excessive current flow has made 3C-SiC p-n junctions unsuitable for rectification purposes (in a diode or as a junction in a transistor structure) beyond a few tens of volts reverse bias [10]–[23]. As a result, the electrical characteristics of 3C-SiC transistors reported on substrates suitable for mass production have been extremely limited, and have failed to offer significant advantages over silicon-based technologies [20]–[28]. The only superior 3C-SiC devices reported to date were produced on Acheson furnace crystals, which are not generally considered suitable for mass production [29]–[31].

In 1991 Powell *et al.* reported on a technique for obtaining improved quality 3C-SiC through CVD growth on commercially available 6H-SiC wafers with low tilt-angles [32], [33]. This process produces patterned 1-mm × 1-mm die sized areas of DPB-free reduced stacking fault density epitaxial 3C-SiC on a larger area 6H-SiC wafer. Recently, Larkin *et al.* discovered a new CVD growth technique for silicon carbide [34]. The purpose of this initial communication is to report on the combined use of these techniques to produce greatly improved 3C-SiC p-n junction diodes whose electrical performance shatters that of previously reported 3C diodes fabricated on mass producible substrates.

The 3C-SiC and 6H-SiC epilayers shown in Fig. 1 were grown on commercially available[1] n^+ 6H (0001) silicon-face SiC substrates with tilt angles ranging from 0.2° to 0.3° (where 0° = the [0001] SiC basal plane). Wafer tilt

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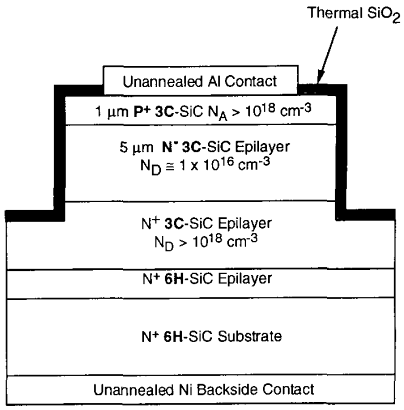

Fig. 1. Cross section of epitaxial 3C-SiC p-n junction diode. 6H-SiC p-n diodes with doping cross sections identical to this figure were also fabricated on 6H epitaxial regions of the same wafer.

angles were measured using an X-ray/laser technique, but tilt direction was not correlated with crystal direction [35]. A series of equally spaced 50-μm-deep grooves were cut into the growth surface of each wafer using a dicing saw, which defined an array of square 1-mm^2 mesas on each wafer. These wafers were used as substrates in subsequent CVD growth, which produced a mixture of 1-mm^2 3C-SiC epilayer mesas and 6H-SiC epilayer mesas on each SiC wafer [32], [33]. To produce the 3C- and 6H-SiC epilayers, silane (3% in H_2) and propane (3% in H_2) were flowed into an atmospheric pressure CVD reactor using a carrier gas of ultrapurified hydrogen. These precursor gases subsequently pyrolyzed on the 6H-SiC substrates which were heated to 1450°C via an inductively heated, SiC-coated graphite susceptor. The positional distribution of 3C epilayer mesas versus 6H epilayer mesas on the wafer was random, and the percentage of 3C mesas was roughly 50%. During the CVD growth process, p-type epilayers were produced by the introduction of trimethylaluminum (via a bubbler configuration) whereas a flow of nitrogen (100 ppm in H_2) was used for n-type epilayer formation. The carrier concentrations of the lightly doped n-type epilayers were measured to be near 1×10^{16} cm^{-3} for both polytypes by CV profiling the finished p-n junction diodes.

A 2000-Å-thick aluminum etch mask defining circular and square diode mesas ranging in area from 7×10^{-6} to 4×10^{-4} cm^2 was applied and patterned by lift-off. The diode mesas were etched to a depth of approximately 10 μm using reactive ion etching (RIE) in 80% SF_6:20% O_2 under 300-W RF at a chamber pressure of 250 mtorr. The aluminum etch mask was stripped by wet etch, and then a cleanup dip in boiling sulfuric acid was performed. The samples were wet oxidized for 6 h at 1150 °C to form SiO_2 at least 500 Å thick [36]. After the wafers had been patterned for contacts, vias were etched in the oxide using 6:1 buffered HF solution. Aluminum was then e-beam deposited and lifted off to complete device fabrication.

Although the growth technique produces regions of 3C epilayers and 6H epilayers on any given wafer, identification of each device's polytype was easily facilitated by the different oxidation rates of the 3C and 6H polytypes [36]. The observed oxide color difference resulting from the 3C and 6H oxide thickness difference clearly distinguished 3C devices from 6H devices on each wafer [36], [37]. Furthermore, the oxidation also delineated stacking faults and DPB's present on the 3C regions of each wafer [37]. Most 3C mesas were free of DPB's. The stacking fault densities varied from mesa to mesa, but the density was significant enough that every 3C device measured contained at least one stacking fault. When placed under sufficient forward bias, the 3C diodes emitted light that was visually observed to range in color from yellow to green. Diodes in the 6H regions emitted light visually ranging from blue to violet, and had notably different electrical characteristics than diodes in the 3C regions of the wafers. The electrical characteristics of the 6H diodes will not be discussed in this communication, except to say that they were very similar to those previously reported in [38].

Fig. 2 shows the current–voltage characteristic obtained from a representative 3C-SiC p-n junction diode at room temperature. The 3C diode exhibits rectification to 200-V reverse bias, which represents a fourfold improvement in 3C-SiC diode voltage handling capability [10]–[23]. The breakdown is repeatable (i.e., the curve can be taken numerous times with no change in device characteristics) when the current flowing during reverse breakdown is restricted to less than 1 mA; unlimited current flow results in permanent damage to the diode. On all the devices tested on this wafer, coronas of microplasmas were observed exclusively around device boundaries during breakdown suggesting that reverse failures are occurring at the mesa perimeter and are not due to a bulk mechanism. Once a diode had been catastrophically damaged by excessive current flow during breakdown, the multi-microplasma corona was replaced by a single microplasma which presumably was the point of catastrophic device failure along the mesa edge.

Fig. 3 details the forward and reverse current–voltage characteristics on a logarithmic scale at several temperatures. Although the improvement in reverse leakage naturally depends upon the voltage and temperature selected as a basis of comparison, these 3C-SiC diodes clearly represent at least an order of magnitude improvement in reverse leakage current density over any previously published 3C-SiC p-n diode [10]–[23]. Because the reverse current is not proportional to the square root of the applied voltage, it is surmised that mechanisms other than thermal generation are responsible for the reverse leakages. The exponential regions of the forward characteristics exhibit record-low saturation current densities (Fig. 3) for CVD-grown 3C p-n diodes [10]–[18], [21]–[23]. However, the ideality factor change with temperature is not well-understood at this time. As confirmed by measurements on contact test structures, the nonexponential behavior limiting the forward current at biases above 1.3 V

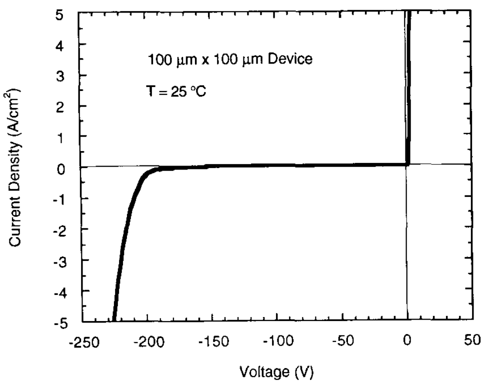

Fig. 2. Room-temperature current–voltage characteristics of a typical 3C SiC p-n diode. The rectification out to −200 V represents a fourfold improvement in 3C SiC diode blocking voltage. The diodes exhibited significantly bright green–yellow light emission when forward biased.

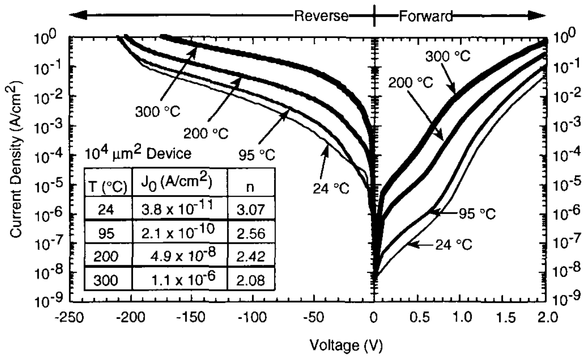

Fig. 3. Semi-logarithmic plots of forward and reverse I–V characteristics at several temperatures. Note the difference in the horizontal voltage scale between forward and reverse voltages. The inset table gives the saturation current densitites (J_0's) and ideality factors (n's) computed from the exponential regions of the forward-biased curves. The forward current at higher voltages (~ 1.3 V and above) was limited by a parasitic Schottky barrier formed between the p^+ cap layer and the unannealed top aluminum contact.

in Fig. 3 is due to the parasitic reverse-biased Schottky barrier formed between the unannealed top aluminum contact and the p^+ cap layer.

Though this work represents a vast improvement in CVD-grown 3C-SiC produced on readily available substrates, it is the authors' opinion that substantial room for advancement remains. It is surmised that the stacking faults or other defects still present in the 3C epilayers may dominate some of the electrical characteristics, but this is still being studied. In spite of the remaining challenges, however, the new 3C-SiC epitaxial growth techniques [32]–[34] should enable substantial improvements in the performance (especially in the areas of reduced parasitic leakages and increased voltage handling capabilities) of most 3C-SiC transistors. Experiments investigating potential improvements in reproducible 3C carrier mobilities, which would also enhance transistor performance, are being undertaken.

In summary, greatly improved CVD-grown 3C-SiC p-n junction diodes have been fabricated on commercially available substrates. These diodes demonstrate the first reported 3C-SiC rectification to 200 V, and exhibit substantial improvements in reverse leakage and forward saturation current densities over previously reported 3C-SiC diodes produced on commercially available wafers. Application of this CVD growth technique to transistor structures should lead to significant advancements in 3C-SiC device and circuit performance and capabilities.

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References

[1] R. F. Davis, G. Kelner, M. Shur, J. W. Palmour, and J. A. Edmond, "Thin film deposition and microelectronic and optoelectronic device fabrication and characterization in monocrystalline alpha and beta silicon carbide," *Proc. IEEE*, vol. 79, no. 5, pp. 677–701, 1991.

[2] P. A. Ivanov and V. E. Chelnokov, "Recent developments in SiC single-crystal electronics," *Semiconductor Sci. Technol.*, vol. 7, pp. 863–880, 1992.

[3] J. A. Powell, P. G. Neudeck, L. G. Matus, and J. B. Petit, "Progress in silicon carbide semiconductor technology," in *Mat. Res. Soc. Symp. Proc.*, vol. 242, 1992, pp. 495–505.

[4] R. J. Trew, J. B. Yan, P. M. Mock, "The potential of diamond and SiC electronic devices for microwave and millimeter-wave power applications," *Proc. IEEE*, vol. 79, no. 5, pp. 598–620, May 1991.

[5] B. J. Baliga, "Impact of SiC on power devices," in *Amorphous and Crystalline Silicon Carbide IV*, C. Y. Yang, M. M. Rahman, and G. L. Harris, Eds. Berlin: Springer-Verlag, 1992, pp. 305–313.

[6] M. G. Spencer, "The prospects for beta silicon carbide materials and devices," in *Proc. 1991 Int. Semiconductor Device Res. Symp.* (Charlottesville, VA), 1991, pp. 503–504.

[7] C. M. Chorey, P. Pirouz, J. A. Powell, and T. E. Mitchell, "The investigation of β-SiC epitaxially on Si substrate by CVD," in *Semiconductor-Based Heterojunctions: Interfacial Structure and Stability*, M. L. Green, J. E. E. Baglin, G. Y. Chin, H. W. Deckman, W. Mayo, and D. Narasinham, Eds. Warrendale, PA: Metallurgical Society, 1986, pp. 115–125.

[8] S. R. Nutt, D. J. Smith, H. J. Kim, and R. F. Davis, "Interface structures in beta-silicon carbide thin films," *Appl. Phys. Lett.*, vol. 50, no. 4, pp. 203–205, 1987.

[9] P. Pirouz, C. M. Chorey, and J. A. Powell, "Antiphase boundaries in epitaxially grown β-SiC," *Appl. Phys. Lett.*, vol. 50, no. 4, pp. 221–223, 1987.

[10] R. W. Bartlett and R. A. Mueller, "Epitaxial growth of β-SiC," *Mat. Res. Bull.*, vol. 4, pp. S 341–354, 1969.

[11] S. Nishino, H. Suhara, and H. Matsunami, "Reproducible preparation of cubic-SiC single crystals by chemical vapor deposition," in *Extended Abstr. 15th Conf. Solid State Devices and Mater.*, 1983, pp. 317–320.

[12] K. Furukawa, A. Uemoto, M. Shigeta, A. Suzuki, and S. Nakajima, "3C-SiC P-N junction diodes," *Appl. Phys. Lett.*, vol. 48, no. 22, pp. 1536–1537, 1986.

[13] A. Suzuki, A. Uemoto, M. Shigeta, K. Furukawa, and S. Nakajima, "High-temperature characteristics of CVD-Grown β-SiC p-n junction diodes," in *Extended Abstr. 18th Int. Conf. Solid State Devices and Mater.*, 1986, pp. 101–104.

[14] H. J. Kim and R. F. Davis, "Theoretical and empirical studies of impurity incorporation into β-SiC thin films during epitaxial growth," *J. Electrochem. Soc.*, vol. 133, no. 11, pp. 2350–2357, 1986.

[15] S. Nishino, H. Suhara, H. Ono, and H. Matsunami, "Epitaxial growth and electric characteristics of cubic SiC on silicon," *J. Appl. Phys.*, vol. 61, no. 10, pp. 4889–4893, 1987.

[16] R. E. Avila, J. J. Kopanski, and C. D. Fung, "Behavior of ion-implanted junction diodes in 3C SiC," *J. Appl. Phys.*, vol. 62, no. 8, pp. 3469–3471, 1987.

[17] H. Matsunami, "Highly mismatched hetero-epitaxial growth of cubic SiC on Si," in *Mat. Res. Soc. Symp. Proc.*, vol. 97, 1987, pp. 171–182.

[18] J. A. Edmond, K. Das, and R. F. Davis, "Electrical properties of ion-implanted p-n junction diodes in β-SiC," *J. Appl. Phys.*, vol. 63, no. 3, pp. 922–929, 1988.

[19] V. L. Zuev and E. I. Rybina, "Current–voltage characteristics of diffused structures in β-SiC," *Sov. Phys. Semicond.*, vol. 11, no. 9, pp. 1056–1058, 1977.

[20] S. Kaneda, Y. Sakamoto, T. Mihara, and T. Tanaka, "MBE growth of 3C-SiC/6H-SiC and the electrical properties of its p-n junction," *J. Cryst. Growth*, vol. 81, pp. 536–542, 1987.

[21] K. Shibahara, T. Takeuchi, T. Saitoh, S. Nishino, and H. Matsunami, "Inversion-type MOS field effect transistors using CVD grown cubic SiC on Si," in *Mat. Res. Soc. Symp. Proc.*, vol. 97, 1987, pp. 247–252.

[22] S. Yoshida *et al.*, "Electrical properties of 3C-SiC and its application to FET," in *Mat. Res. Soc. Symp. Proc.*, vol. 97, 1987, pp. 259–264.

[23] H. Kong *et al.*, "Growth, doping, device development and characterization of CVD beta-SiC epilayers on Si(100) and alpha-SiC(0001)," in *Mat. Res. Soc. Symp. Proc.*, vol. 97, 1987, pp. 233–245.

[24] Y. Kondo *et al.*, "Experimental 3C-SiC MOSFET," *IEEE Electron Device Lett.*, vol. EDL-7, no. 7, pp. 404–406, 1986.

[25] K. Furukawa *et al.*, "Insulated-gate and junction gate FET's of CVD-grown β-SiC," *IEEE Electron Device Lett.*, vol. EDL-8, no. 2, pp. 48–49, 1987.

[26] G. Kelner, S. Binari, K. Sleger, and H. Kong, "β-SiC MESFETs," *Mat. Res. Soc. Symp. Proc.*, vol. 97, 1987, pp. 227–231.

[27] H. S. Kong, J. W. Palmour, J. T. Glass, and R. F. Davis, "Temperature dependence of the current–voltage characteristics of metal–semiconductor field-effect transistors in n-type β-SiC grown via chemical vapor deposition," *Appl. Phys. Lett.*, vol. 51, no. 6, pp. 442–444, 1987.

[28] A. Suzuki, K. Furukawa, Y. Fujii, M. Shigeta, and S. Nakajima, "Crystal growth of β-SiC on Si and its application to MOSFET's," in *Amorphous and Crystalline Silicon Carbide III and Other Group IV–IV Materials*, G. L. Harris, M. G. Spencer, and C. Y. Yang, Eds. Berlin: Springer-Verlag, 1992, pp. 101–110.

[29] J. W. Palmour, H. S. Kong, and R. F. Davis, "High-temperature depletion-mode metal–oxide–semiconductor field-effect transistors in beta-SiC thin films," *Appl. Phys. Lett.*, vol. 51, no. 24, pp. 2028–2030, 1987.

[30] H. S. Kong, J. T. Glass, and R. F. Davis, "Epitaxial growth of β-SiC thin films on 6H α-SiC substrates via chemical vapor deposition," *Appl. Phys. Lett.*, vol. 49, no. 17, pp. 1074–1076, 1986.

[31] J. W. Palmour, H. S. Kong, and R. F. Davis, "Characterization of device parameters in high-temperature metal–oxide–semiconductor field-effect transistors in β-SiC thin films," *J. Appl. Phys.*, vol. 64, no. 4, pp. 2168–2177, 1988.

[32] J. A. Powell *et al.*, "Controlled growth of 3C-SiC and 6H-SiC on low-tilt-angle vicinal (0001) 6H-SiC wafers," *Appl. Phys. Lett.*, vol. 59, no. 3, pp. 333–335, 1991.

[33] J. A. Powell, D. J. Larkin, J. B. Petit, and J. H. Edgar, "Investigation of the growth of 3C-SiC and 6H-SiC films on low-tilt-angle vicinal (0001) 6H-SiC wafers," in *Amorphous and Crystalline Silicon Carbide IV*, C. Y. Yang, M. M. Rahman, and G. L. Harris, Eds. Berlin: Springer-Verlag, 1992, pp. 23–30.

[34] D. J. Larkin, P. G. Neudeck, J. A. Powell, and L. G. Matus, paper in preparation.

[35] J.-W. Yang, P. Pirouz, and J. A. Powell, unpublished work.

[36] J. B. Petit, P. G. Neudeck, L. G. Matus, and J. A. Powell, "Thermal oxidation of single-crystal silicon carbide: Kinetic, electrical, and chemical studies," in *Amorphous and Crystalline Silicon Carbide IV*, C. Y. Yang, M. M. Rahman, and G. L. Harris, Eds. Berlin: Springer-Verlag, 1992, pp. 190–196.

[37] J. A. Powell *et al.*, "Application of oxidation to the structural characterization of SiC epitaxial films," *Appl. Phys. Lett.*, vol. 59, no. 2, pp. 183–185, 1991.

[38] L. G. Matus, J. A. Powell, and C. S. Salupo, "High-voltage 6H-SiC P-N junction diodes," *Appl. Phys. Lett.*, vol. 59, no. 14, 1991.